STAR CMOS KEYER

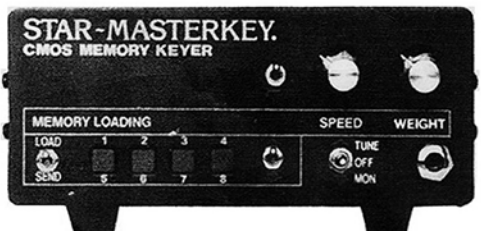


Fig.1 Front panel of the keyer, with toggle switches set prior to clearing memories.

In these days of oriental domination of the Amateur market it is rare to see a British made unit which competes not only in performance but also in appearance and price too. Some months ago, Tony Dewsbury started making the Star Masterkey which gives operating instructions in some details, but does not *(unfortunately — Ed.)* include a circuit diagram.

The keyer retains all of the features of the basic Masterkey and adds no less than eight memories,

There are a few home-grown alternatives to imported electronic morse keyers — Dave Reynolds, G3ZPF, takes the Dewsbury memory keyer for a test run.

which proved popular from the moment it was introduced. It was inevitable that a memory version would follow, and recently I was asked to put it through its paces for 'Ham Radio Today'.

The unit comes in packaging which should survive the rigours of the postal system with ease, and first impressions on opening it were how smart it looked in its black and gold livery. The appearance of a fairly simple case has been improved dramatically by the addition of a screen printed front plate. An A5 handbook is supplied with the unit each of which can store about 50 characters. The precise number of characters which can be stored will depend on the message as the length of morse characters varies, but the quoted figure seems a realistic estimate.

The unit measures 153mm wide x 78mm high x 197mm deep, and is supplied with four AA batteries already fitted. Sidetone is variable in both pitch and amplitude, and the keyer will operate rigs with either direct or grid block keying which makes it suitable for either solid state rigs such as the TS930, or valve rigs like the Yaesu FT101ZD. As supplied the speed range is from 7 to 42 words per minute (wpm).

Initial Setting Up

On obtaining one of these keyers, the first thing to do is flush the memories of any odd characters which may be stored in them. After this has been done, reset the speed control to the normal setting and press the desired memory button. Memory scanning will start at once, so start keying your message straight away or you will lose space. In the LOAD position morse input is not transmitted while the memory is loaded.

If you complete your message before the LED goes out, wait until it does before moving on to the next memory. I was rather dubious about not knowing exactly when the memory would be filled, until it had, but after practicing with it for a while I soon got used to it. After loading the memories as necessary do not forget to put the toggle switch in the SEND position before selecting memories again, or the contents will be lost. Sounds obvious? Yours truly erased messages more times than he cares to remember initially.

In the SEND position any keyed morse will be transmitted and memories can be transmitted simply by pressing the appropriate red button. Memory transmission can be halted at any time by momentarily pressing the paddle. To give an example of what can be stored in the memories, the following were programmed by myself while testing the keyer.

(1) CQ CQ CQ CQ DE G3ZPF G3ZPF G3ZPF AR K
(2) NAME DAVID DAVID QTH NR DUDLEY NR DUDLEY
(3)RIG TS930 TS930 ES ANT INV VEE INV VEE APEX 30 FEET
(5) TEST TEST DE G3ZPF G3ZPF .

Fig. 2 Rear view showing keying sockets for solid state and valve rigs, together with headphone jack. The two holes at the bottom right give access to presets to adjust sidetone pitch and volume.

G3ZPF TEST TEST TEST DE G3ZPF TEST

The reason for putting the 'test' message in memory 5 is that with the auto character space switched on, memories 1 and 5 will repeat endlessly until the paddle is pressed momentarily. Auto character spacing is selected by the toggle switch to the left of the speed control.

In Use

One of the first things I discovered when trying out the keyer was how rusty I had become as I now exclusively use a straight key. Consequently a good deal of time was spent off-air getting used to it before venturing on to the bands. It keyed my TS930 and TS520 perfectly, and seriously tempted me to give up using a straight key for good. The only problems with sending were all due to myself, and I can thoroughly recommend this unit to anyone looking for a memory keyer, especially as it is only about 50% of the price of many comparable imported units.

The only criticism I have to make is that it would have been nice to have had a pause facility on memories, to allow insertion of RST into messages for instance, and to have been able to 'chain' memories together for longer messages, but having said that I've yet to come across a keyer that does, apart from microprocessor based devices.

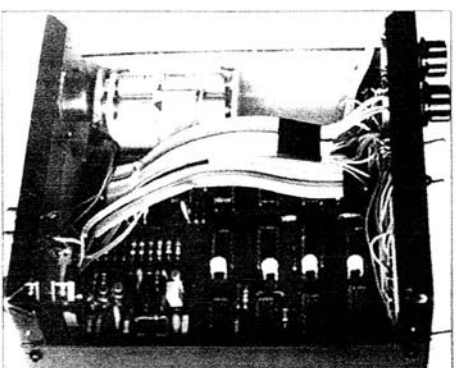


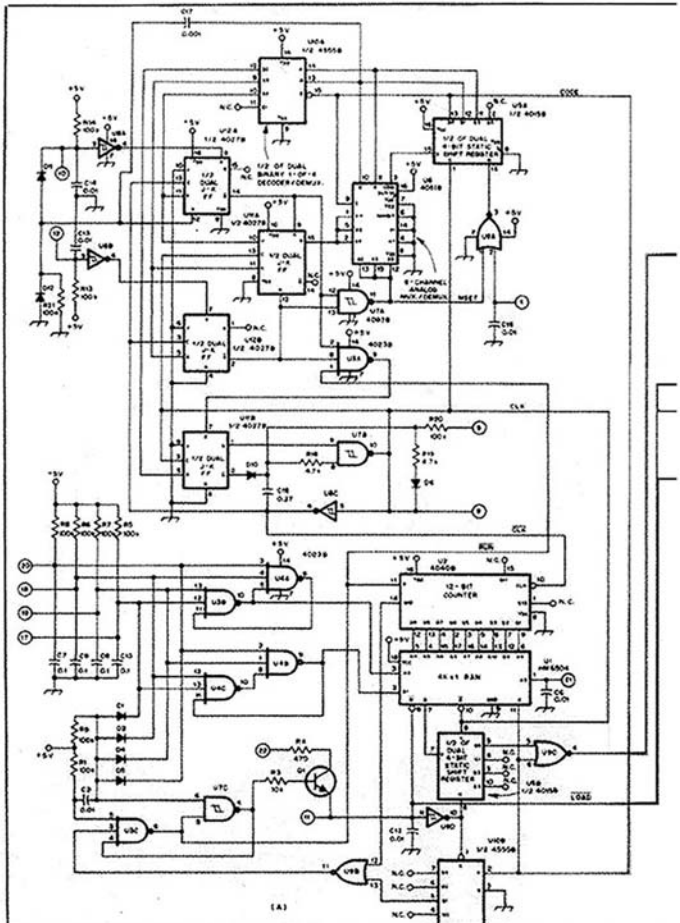
Fig. 3 Internal view of keyer. All components are mounted on a high quality PCB, and main cabling runs use ribbon cable for neatness. The wiring harness is arranged to allow the board to be removed for servicing whilst still connected.

Comments

This model does not supersede the original keyer, which continues to be produced at £54.70. Those readers requiring the extra facilities of the CMOS Memory Keyer will need to find £95.00 incl, with p&p for both devices being £3 extra.

You will also need a paddle unit to go with these keyers, and a variety can be obtained, varying from £17 to about £120 (!!).

I would like to thank Dewsbury Electronics of Stourbridge, for supplying the review unit.



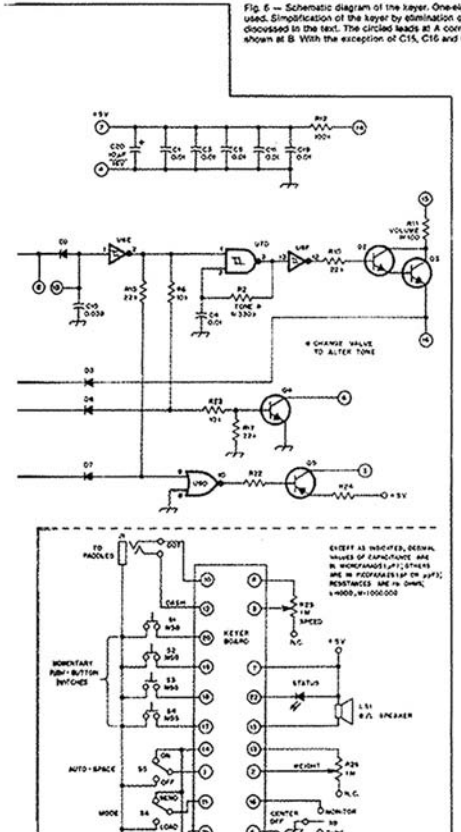


Fig. 6 — Schematic diagram of the keyer. One-eighth- or ¼-watt carbon resistors should be used. Simplification of the keyer by elimination of features and by component selection is discussed in the text. The circled leads at A correspond to the board edge connector pads shown at B. With the exception of C15, C16 and C20, all capacitors are disc ceramic, 50-V units.

C15 — Mylar, 0.039 μF, 50 V.
C16 — Mylar, 0.27 μF, 50 V.
C20 — Electrolytic or tantalum, 10 μF, 10 V.
D1-D12, incl. — Silicon, fast-switching diode, 100 PIV, 75 mA, 4 ns, 1N4454, 1N914, 1N4148 or equiv.
Q1-Q3, incl. — NPN silicon low power, general-purpose amplifier, 500 mW, 2N2222 or equiv.
Q4-Q5 — See text.
U1 — CMOS 4K x 1 RAM, Harris HM6504-9
U2 — CMOS 12-bit counter, 4040B.
U3,U4 — CMOS triple 3-input nand gate, 4023B.
U5 — CMOS dual shift register, 4015B.
U6 — CMOS 8-to-1 multiplexer, 4051B.
U7 — CMOS quad Schmitt nand gate, 4093B.
U8 — CMOS hex Schmitt inverter, 40106D, MC14585B.
U9 — CMOS quad 2-input nor gate, 4001B
U10 — CMOS dual 2-to-4 decoder, 4555B.
U11,U12 — CMOS dual J-K FF, 4027B.

dash memories; (9) has switch-selectable, auto-character spacing; (10) uses a gated clock for instantaneous asynchronous starting; (11) has ultra-low power requirements; (12) features continuous message retention; (13) offers very friendly timing circuitry.

Those interested in logic design will find this presentation useful and interesting. Several novel features help to reduce the chip count — only 12 readily available ICs are required. CMOS devices are employed, and with no quiescent current paths the keyer draws only 10 to 15 microamperes in standby. It has no on/off switch! A state transition diagram is also included.

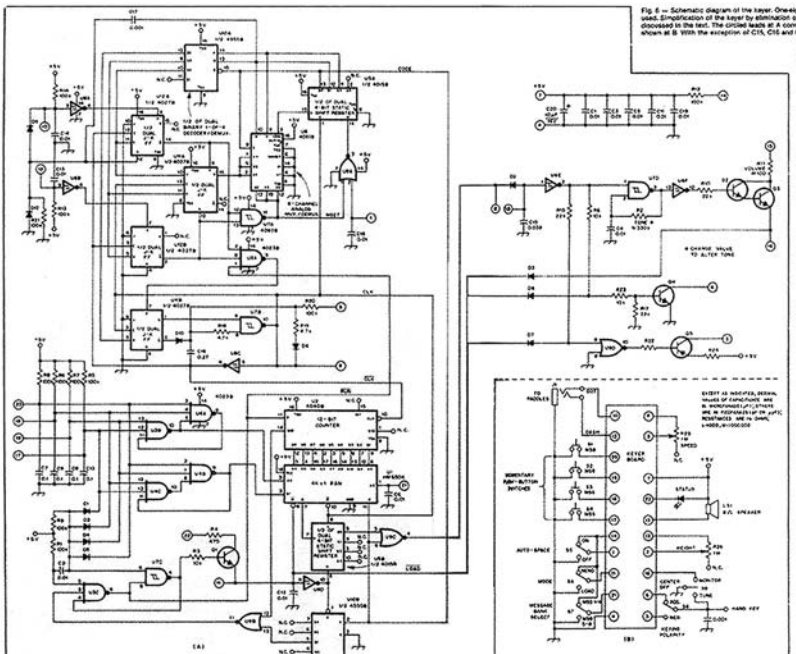
Cost

Certainly this is a factor of primary concern to amateurs. Total IC costs will be about $10, including an approximate cost of $7 for the RAM chip. A helpful junk box should lower construction costs to less than $25. If all components are purchased new, anticipate a $60 price tag.

CMOS Design

Fig. 6 shows the schematic diagram of the CMOS Super Keyer. The advantages of CMOS technology are apparent in this keyer: low cost, ultra-low power requirements, wide logic swings, "down-the-middle" transfer characteristics, high impedance inputs, lots of "fan out" drive capability and good noise immunity, to name a few. The 6504 RAM can store 4096 bits: that's eight messages of 512 bits each, or about 50 characters per message.

This circuit does not depend on how fast one IC is with respect to another. In some designs you are instructed to swap this or that IC if you have a problem, or RC networks are added to the circuit to reduce "glitches" or race conditions. There is no need for RC de-glitchers in this design. The read-in/read-out memory-address transitions are logically synchronized, and all



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